IN THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) For use in a shared bus system comprising a plurality of bus devices capable of requesting access to a shared bus, a bus arbitrator operable to slowly activate and rapidly de-activate tristate line drivers coupled to said shared bus, said bus arbitrator comprising:

an input circuit ~~interface~~ capable of receiving a first bus access request signal from a first of said plurality of bus devices and a second bus access request signal from a second of said plurality of bus devices, the input circuit also capable of outputting the second bus access request signal when the first bus access request signal is not enabled and blocking the second bus access request signal when the first bus access request signal is enabled;

a delay circuit capable of receiving said first bus access request signal ~~from said input interface~~ and generating therefrom a time-delayed first bus access request signal; and

a comparator circuit capable of receiving said first bus access request signal ~~from said input interface~~ and said time-delayed first bus access request signal ~~from said delay circuit~~ and generating a line driver enable signal only if both of said first bus access request signal and said time-delayed first bus access request signal are enabled.

2. (Original) The bus arbitrator as set forth in Claim 1 wherein comparator circuit disables said line driver enable signal if either of said first bus access request signal and said time-delayed first bus access request signal is disabled.

3. (Original) The bus arbitrator as set forth in Claim 2 wherein a time delay of said delay circuit is greater than a maximum de-activation delay period associated with said tri-state line drivers.

4. (Original) The bus arbitrator as set forth in Claim 3 wherein said comparator circuit comprises an AND gate having a first input for receiving said first bus access request and a second input for receiving said time-delayed first bus access request signal.

5. (Original) The bus arbitrator as set forth in Claim 3 wherein said delay circuit is an asynchronous delay circuit.

6. (Currently Amended) The bus arbitrator as set forth in Claim 5 wherein said delay circuit comprises an even number of inverters connected in series, wherein a first of said even number of inverters receives said first bus access request signal ~~from said input interface~~ and a last of said even number of inverters generates said time-delayed first bus access request signal.

7. (Original) The bus arbitrator as set forth in Claim 3 wherein said delay circuit is a synchronous delay circuit.

8. (Currently Amended) The bus arbitrator as set forth in Claim 7 wherein said delay circuit comprises a flip-flop having an input capable of receiving said first bus access request signal ~~from said input interface~~ and an output coupled to said comparator circuit that generates said time-delayed first bus access request signal.

9. (Currently Amended) A shared bus system comprising:

N bus devices capable of requesting access to a shared bus;

M tristate line drivers, each of said M tristate line drivers having an input for receiving a logic bit from one of said N bus devices and an output for outputting said received logic bit to said shared bus, wherein said each tristate line driver outputs said received logic bit when a line driver enable signal associated with said each tristate line driver is enabled and an output of said each tristate line driver is put into a high-impedance state when said line driver enable signal is disabled; [[and]]

a bus arbitrator operable to slowly activate and rapidly de-activate said M tristate line drivers, said bus arbitrator comprising:

an input interface capable of receiving a first bus access request signal from a first of said N bus devices;

a delay circuit capable of receiving said first bus access request signal from said input interface and generating therefrom a time-delayed first bus access request signal; and

a comparator circuit capable of receiving said first bus access request signal from said input interface and said time-delayed first bus access request signal from said delay circuit and generating a line driver enable signal only if both of said first bus access request signal and said time-delayed first bus access request signal are enabled; and

a bus keeper capable of holding each line of the shared bus at a particular logic level when all of the tristate line drivers are put into the high-impedance state.

10. (Original) The shared bus system as set forth in Claim 9 wherein comparator circuit disables said line driver enable signal if either of said first bus access request signal and said time-delayed first bus access request signal is disabled.

11. (Original) The shared bus system as set forth in Claim 10 wherein a time delay of said delay circuit is greater than a maximum de-activation delay period associated with said tri-state line drivers.

12. (Original) The shared bus system as set forth in Claim 11 wherein said comparator circuit comprises an AND gate having a first input for receiving said first bus access request and a second input for receiving said time-delayed first bus access request signal.

13. (Original) The shared bus system as set forth in Claim 11 wherein said delay circuit is an asynchronous delay circuit.

14. (Original) The shared bus system as set forth in Claim 13 wherein said delay circuit comprises an even number of inverters connected in series, wherein a first of said even number of inverters receives said first bus access request signal from said input interface and a last of said even number of inverters generates said time-delayed first bus access request signal.

15. (Original) The shared bus system as set forth in Claim 11 wherein said delay circuit is a synchronous delay circuit.

16. (Original) The shared bus system as set forth in Claims 15 wherein said delay circuit comprises a flip-flop having an input capable of receiving said first bus access request signal from said input interface and an output coupled to said comparator circuit that generates said time-delayed first bus access request signal.

17. (Currently Amended) For use in a shared bus system comprising N bus devices capable of requesting access to a shared bus, a method for slowly activating and rapidly de-activating a plurality of tristate line drivers coupled between the shared bus and the N bus devices, the method comprising the steps of:

receiving a first bus access request signal from a first of the ~~plurality of~~ bus devices;

generating from the first bus access request signal a time-delayed first bus access request signal; [[and]]

comparing in a comparator circuit the first bus access request signal and the time-delayed first bus access request signal and generating a line driver enable signal only if both of the first bus access request signal and the time-delayed first bus access request signal are enabled; and

holding each line of the shared bus at a particular logic level when all of the tristate line drivers are put into a high-impedance state.

18. (Original) The method as set forth in Claim 17 further comprising the step of disabling the line driver enable signal if either of the first bus access request signal and the time-delayed first bus access request signal is disabled.

19. (Original) The method as set forth in Claim 18 wherein a time delay associated with the time-delayed first bus access request signal is greater than a maximum de-activation delay period associated with the plurality of tri-state line drivers.

20. (Currently Amended) The ~~shared bus system~~ method as set forth in Claim 19 wherein the comparator circuit comprises an AND gate having a first input for receiving the first bus access request and a second input for receiving the time-delayed first bus access request signal.

21. (New) The bus arbitrator of Claim 1, wherein the input circuit comprises:

an inverter capable of receiving and inverting the first bus access request signal; and

an AND gate capable of receiving the inverted first bus access request signal and the second bus access request signal, the AND gate also capable of outputting the second bus access request signal when the first bus access request signal is not enabled and blocking the second bus access request signal when the first bus access request signal is enabled.